REMARKS/ARGUMENTS

Claims 1-24, 26-29, 32-36, and 38 as amended through the above claim amendments, along with new claims 39-40, are currently pending in the present patent application. Claims 30, 31 have been cancelled through the above claim amendments and claims 25 and 37 cancelled through prior amendments.

In a final Office Action mailed November 14, 2007, the Examiner maintains his rejections of all pending claims. Specifically, in Section 5 the Examiner explains his interpretation of U.S. Patent No. 6,308,311 to Carmichael *et al.* ("Carmichael"). The Examiner explains that, with reference to Figure 3 of Carmichael, he has interpreted the interface device 30 of Carmichael to be the programmable circuit of the claimed invention. See Section 5 of the Office action. The Examiner points to the cited programmable logic integrated circuit as corresponding to the FPGA 32, the SRAM 36 and SPROM 38 as corresponding to the recited firmware memories, and the address bus 33, control bus 35, USB port connection 40 and serial port connection 42 as corresponding to the recited interface to an outside device. The Examiner expressly points out that signal lines 48 and target FPGA 10 are not relied upon in order for Carmichael to read on the claimed invention and thus are not part of the Examiner's rejections. With regard to the term "interface" recited in claim 1, the examiner states that the connection point between the buses 33 and 35 and the FPGA 32 is the interface. With regard to claim 16, the Examiner states that the specification does not define the term "industry-standard bus" and concludes, therefore, that any bus or wider that is used to connect to peripherals could reasonably be considered an industry-standard bus.

The claims of the present application have been amended in an attempt to address some of the Examiner's comments and his rejections of the claims. Amended claim 1 recites a programmable logic integrated circuit operable to function as an end point on an industry standard bus. The programmable logic integrated circuit includes an interface to the industry standard bus and is operable through the interface to receive multiple versions of firmware from an external source, each version of firmware representing a corresponding operating configuration, store the multiple versions of firmware in a memory, download a selected one of the versions of firmware from the memory, and configure itself using the downloaded firmware to operate in the corresponding operating configuration.

Carmichael neither discloses nor suggests the structure recited in amended claim 1. The claim now recites that the programmable logic integrated circuit is operable to function as an endpoint on an industry-standard bus. An endpoint is "a mark of termination or completion." See Wikipedia, for example. From the description of the pipeline circuit 80 set forth in the present application, it is seen that in the embodiment of Figure 4 such a pipeline circuit is an endpoint on an industry-standard bus since the pipeline circuit performs calculations via the hardwired pipelines 74 and the results of such calculations are communicated from the pipeline circuit through the industry standard bus interface 91.

In Carmichael, neither the interface device 30 nor the FPGA 32 corresponds to an endpoint as recited in amended claim 1. The interface device 30 is, as its name implies, an interface between the host system 20 and target FPGA 10 and is not an endpoint. Therefore, even if the Examiner's interpretation of Carmichael is accepted and the FPGA 32 is assumed to correspond to the recited programmable logic integrated circuit, this FPGA is clearly not an endpoint on an industry-standard bus.

Furthermore, amended claim 1 recites that the programmable logic integrated circuit includes an interface to the industry standard bus. In the embodiment of Figure 4, this corresponds to the industry-standard bus interface 91. The term "industry-standard bus" will be understood by those skilled in the art to be a widely used bus having an associated physical structure and corresponding communications protocol that devices connected to the bus must have in order to communicate over the bus. The Examiner states that the claims do not limit the term industry-standard bus to a structure that is anything more than a single wire. This focuses only on the physical aspect of a bus and ignores the associated communications protocol of the bus. The term "bus" includes both the physical structure and the associated communications protocol, with these two terms together defining a given bus. An industry standard bus is a widely used bus having the associated physical structure and communications protocol, such as a USB bus or a Rapid I/O bus.

In Carmichael, the FPGA 32 does not include an interface to an industry-standard bus. Instead, this is the function of the microcontroller 34 and USB and serial connections 40 and 42. The control bus 35 and address bus 33 do not together form an industry standard bus, which is the reason the microcontroller 34 is required, namely to interface industry-standard buses in the form of the USB connection 40 and serial connection 42 to the FPGA 32. If the control bus 35 address bus 33 were an industry-standard bus, then

the host system 20 could simply communicate over such a bus directly with the FPGA 32, which would correspond to the structure recited in claim 1. In Carmichael, this is clearly not the case as expressly shown in Figure 3.

For all these reasons, the combination of elements recited in amended claim 1 is allowable. Dependent claims 2-6 are allowable for at least the same reasons as claim 1 and due to the additional limitations added by each of these claims.

Independent claims 5, 7 and 10 are allowable for reasons similar to those just discussed with regard to claim 1, and the associated dependent claims 6, 8, 9, and 11-12 are allowable for at least the same reasons as the

Claims 6 and 11 recite "the second firmware version may only be received when operating in the first configuration." The Examiner points to column 7, lines 58-60 of Carmichael as disclosing this recited element. This section of Carmichael merely describes how the microcontroller 34 operates in combination with the FPGA 32 to reconfigure the FPGA. This does not disclose that the FPGA 32 may only reconfigure itself with a second firmware version when the FPGA 32 is operating in a first configuration corresponding to a first firmware version. For these additional reasons, claims 6 and 11 are allowable.

Amended claim 13 recites a programmable-circuit unit including a memory operable to store a plurality of firmware configurations, each firmware configuration respectively representing a corresponding operational configuration. A first programmable logic integrated circuit is coupled to the memory and includes an industry standard interface. The first programmable logic integrated circuit is operable to receive the firmware configurations via the industry standard bus and to store these configurations in the memory. A second programmable logic integrated circuit is coupled to the memory and to the first programmable circuit. One embodiment covered by claim 13 is illustrated in Figure 6 of the present application.

Claim 13 was rejected over the combination of Carmichael and U.S. Patent Application Publication No. 2003/0177223 to Erickson ("Erickson"). Erickson is directed to a computer version checking system while Carmichael is directed to a system for reconfiguring FPGAs 10. Even if combined, the resulting combination does not disclose a first programmable logic integrated circuit including an industry standard interface that receives firmware configurations via an industry standard bus and stores these

configurations in a memory and a second programmable logic integrated circuit coupled to the first and to the memory. The Examiner states it would have been obvious to modify Carmichael to include multiple FPGAs running different versions of firmware to provide higher computing power. In such a system, why would the multiple FPGAs need to interconnected since they are running in parallel executing respective firmware versions? Claim 13 expressly recites the first and second programmable logic integrated circuits are interconnected. The combination of elements recited in claim 13 is allowable and the associated dependent claims are allowable for at least the same reasons as the claim 13 and due to the additional limitations added by each of these dependent claims.

Independent claims 16, 20 and 24 recite, in part, a programmable logic integrated circuit coupled to the memory, and the programmable logic integrated circuit directly coupled to the industry standard bus and through this bus to the processor. Carmichael neither discloses nor suggests such a direct interconnection of the FPGA 32 since the interconnection between this FPGA and the microcontroller 34 is not an industry standard bus as previously discussed. Claims 16 and 20 are allowable for at least this reason and the associated dependent claims are allowable for at least the same reasons as the claims 16 and 20 and due to the additional limitations added by each of these dependent claims.

Independent 32 claim recites, in part, a method that includes downloading over an industry-standard bus directly into the programmable logic integrated circuit a first firmware code that represents a first configuration. Independent claim 36 recites, in part, downloading over an industry-standard bus a first and a second one of the firmware codes directly into the first and second programmable logic integrated circuits, respectively. These firmware codes are downloaded directly into the recited programmable logic integrated circuits. Carmichael neither disclose nor suggests such a downloading but instead uses the microcontroller coupled between the industry standard USB and serial buses to communicate with the FPGA 32. For at least this reason, claims 32 and 36 are allowable and the associated dependent claims are allowable for at least the same reasons as the claims 32 and 36 and due to the additional limitations added by each of these dependent claims.

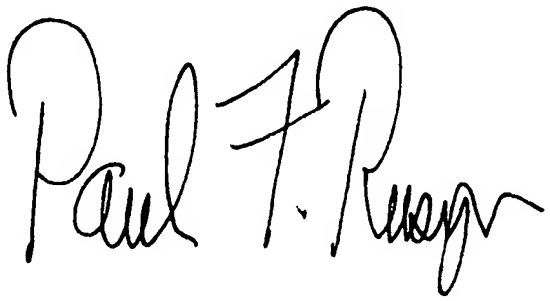
New claim 40 recites the programmable-circuit unit of claim 39 further comprising a router coupled to the pipeline bus. No such structure is disclosed or suggested in

Carmichael or the other references of record and this claim is allowable for these additional reasons.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to resolve the matter. If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP



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